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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,691	11/20/2001	Daniel William Bailey	1662-37600 JMH (P00-3208)	9010

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,691	BAILEY, DANIEL WILLIAM	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,11-22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-22 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 5/2/05 in which claims 1-7, 11-22 and 24-36 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 11-22, 24 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donnely et al U.S patent No 5,945,862 in view of Gaudet U.S. Patent No 6,094,082.

As per claim 1 and 17, Donnely et al teaches a locked loop system that synchronizes a clocked signal to a reference clock signal, comprising: a phase detector (see fig.5 element 610 and col., lines 33-34) that detects a difference in phase between the clocked signal and the reference clock signal, and generates an output signal indicating the phase difference; a digital counter (see fig.5 element 620 and col.5, lines 36-35) coupled to the phase detector, said digital counter receiving the output signal generated by the phase detector, and in response, modifying its count value and generating a binary output signal indicating said count value; an electronic circuit (see figs. 4-5 element 500) coupled to said digital counter, said electronic circuit being configured to receive said binary output signal, and in response, generate a

thermometer-coded (see fig.10 and col.8, lines 50-60 and col.9, lines 5-16)) output signal that corresponds to said binary output signal; and a delay line coupled to said electronic circuit, said delay line including a plurality of delay elements (see figs.4, 5 elements 410, 510 and col.8, lines 35-55) that are enabled by said thermometer-coded output signal.

However Donnely et al does not teach said electronic circuit comprises comparator logic including a first and second comparators and wherein said first comparator receives said binary output signal from said digital counter and in response generates multiple thresholds values.

Gaudet teaches teach said Delay locked loop circuit comprises comparator logic including a first and second comparators and wherein said first comparator receives said binary output signal from said digital counter and in response generates multiple levels (thresholds) values (see col.6, lines 63-67 and col.8, lines 13-15).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Gaudet in to Donnnely as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claim 2, Donnnely et al does teach wherein the digital locked loop system comprises a digital delay locked loop (see fig.5).

As per claim 3, Donnnely et al does teach, wherein the digital locked loop system comprises a digital phase locked loop (see fig.5).

As per claim 4, Donnnely et al does teach, wherein the clocked signal comprises a feedback clock generated by said delay line, and the reference clock signal comprises a synchronized clock signal (see fig.5).

As per claim 5, Donnnely t et does teach wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal (see col.5, lines 36-40).

As per claim 6, Donnnely et al does teach wherein the digital counter increases its count value in response to the increment count signal, and decreases its count value in response to the decrement clock signal (see col.5, lines 36-40).

As per claim 7, Donnnely et al inherently teach wherein the thermometer-coded output signal includes m output signals, and the binary output signal generated by the digital counter includes x output signals, and wherein the m output signals approximately equals 2.sup.x. (see fig.10 and col.8, lines 50-60 and col.9, lines 5-16).

As per claims 11 and 12 Donnnely et al and Gaudet in combination would teach wherein the second comparator receives said threshold values, and generates said a thermometer-coded output signals as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claim 13, Donnnely et al and Gaudet in combination would teach wherein the binary output signals are transmitted from said digital counter on a plurality of output lines, and wherein the number of output signal lines of said second

comparator exceed the number of output lines of said digital counter as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claim 14, Donnnely et al and Gaudet in combination would teach wherein each of said plurality of logical units has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claim 15, Donnnely et al and Gaudet in combination would teach, wherein each of said plurality of logical units receives at least one of said threshold values from said first comparator, and in response generates a pair of enable signals as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claims 16 and 22, Donnely et al teaches said plurality of delay elements each comprises a transistor stack, and wherein each transistor stack (see fig.15 elements 2130, 3135 and col.9, lines 36-40 Furthermore implementing such teaching to enable signal from associated output line of a second comparator would have been obvious to one skilled in the art as to accurately recover the phase clock in the incoming signal

As per claim 17, Donnnely et al and Gaudet in combination would teach, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claim 18 Donnnely et al and Gaudet in combination would teach wherein said logical unit further includes combinatorial logic (see col.3, lines 26-7). Furthermore implement such teaching to combine together threshold values from said first comparator would have been obvious to one skilled in the art as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

As per claims 20 and 21, Donnnely et al does teach wherein the delay line comprises a plurality of delay elements (see figs.4 elements 410, 510), and wherein each of said second plurality of output signal lines enables one of said plurality of delay elements.

As per claim 24 Donnnely et al does teach wherein the plurality of threshold values are selectively combined to generate the thermometer-coded signal on said second plurality of output signal lines (see fig.10 and col.8, lines 50-60 and col.9, lines 5-16).

As per claim 36, Donnely and Gaudet in combination would teach wherein at least two of said threshold values are compared to generate said thermometer coded

output signal as to recover the data in the recovery block which used a flop in order to clocked the falling and rising edges of the receive signal as taught by Gaudet (see col.6, lines 63-67 and col.8, lines 13-15).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 25-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaudet U.S. patent No 6,094,082.

As per claim 25, Gaudet teaches a digital delay locked loop that controls the amount of delay to apply to a clocked signal to synchronize with a reference signal, comprising: a phase comparator is the same as the claimed (phase detector) that determines (see fig.7 element 110 and col.5, line 23) a difference in phase between the clocked signal and the reference signal, and which generates an output signal that indicates if the clocked signal is ahead of or behind the reference signal; a binary counter (see fig.7 element 116and col.5, lines 28-35) that produces a binary output signal that indicates a desired delay for said clocked signal based on a count value produced in response to said output signal from said phase detector; comparator logic (see col.6, lines 63-67) that establishes threshold values for said binary output signal, and which generates a plurality of enable output signal based on said threshold values; and a delay (see figs. 1, 7 elements 12, 118 and col.4, lines 44-60 and col.5,lines 50-

55) that includes a plurality of transistor stacks arranged in parallel, and wherein each of said plurality of said enable signals controls one of said plurality of transistor stacks to thereby control the amount of delay given to said clocked signal (see fig.7)

As per claim 26, Gaudet teaches wherein the clocked signal produced by said delay line is applied to an input of the phase detector as the clocked signal.

As per claim 27, Gaudet inherently teaches wherein the plurality of enable output signals are provided on a plurality of output signal lines between the comparator logic and the delay line.

As per claim 28, Gaudet teaches, wherein the plurality of enable output signals are encoded on said plurality of output signal lines as a thermometer-coded signal (see col.6, lines 50-67).

As per claim 29, Gaudet t teaches, wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal (see col.7, lines 24-35).

As per claim 30, Gaudet teaches wherein the binary counter increases the count value in response to the increment count signal, and decreases its count value in response to the decrement clock signal (see col.7, 24-35).

As per claim 31, Gaudet t teaches, wherein the comparator logic comprises a plurality of logical units that generate said thermometer-coded output signal on a plurality of output signal lines (see col.6, lines 50-67).

As per claim 32 Gaudet inherently teaches wherein each of said plurality of

logical units has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line.

As per claim 33, Gaudet inherently teaches wherein each of said plurality of logical units receives at least one threshold value, and in response generates a pair of enable signals as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 34, Gaudet inherently teaches, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 35, Gaudet inherently teaches wherein said logical unit further includes combinatorial logic for combining together some of said threshold values would have been obvious to one skilled in the art as to accurately recover the phase clock in the incoming.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gu U.S. patent No 6,901,126 B1 teaches a time division multiplex data.

Staszewski et al U.S. Patent no 6,606,004 B2 teaches a system and method for time dithering.

Staszewski et al US Pub no 20020131538 A1 teaches a method and apparatus for asynchronous clock.

Cho U.S. Patent No 6,005,425 teaches a PLL using pulse PWD.

Unkrich U.S. Patent No 5,206,889 teaches a timing interpolator.

Laksmikumar U.S. Patent No 6,104,228 teaches a phase aligner.

Demuliere et al U.S. Patent No 4,258,33 teaches a frequency synthesizer.

Zrubinsky et al U.S. Patent No 6,181,168 B1 teaches a High-speed phase detector.

Jinbo et al US Pub No 2001/0010670 A1 teaches a storage media.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

7/5/05

EMMANUEL BAYARD
PRIMARY EXAMINER